What is claimed is:

1. A machine-implemented method comprising:

receiving a routing address comprising at least two routing identifiers; and

building a routing matrix to use in determining route identification operations to be performed, the routing matrix identifying one or more of the at least two routing identifiers that are to be used in routing.

2. The method of claim 1, wherein the routing address comprises a destination address, and wherein building the routing matrix comprises comparing the destination address with a source address to identify a difference.

3. The method of claim 2, wherein comparing the destination address comprises:

performing an EXCLUSIVE OR operation of the destination address and the source address to produce an address comparison result; and

checking whether the address comparison result includes one or more non-zero values.

4. The method of claim 3, wherein comparing the destination address comprises using parallel processing to compare the destination address with the source address.

5. The method of claim 4, wherein comparing the destination address comprises using blocks smaller than a length of a shortest of the two or more routing identifiers.

6. The method of claim 5, wherein the blocks comprise four-bit blocks.

7. The method of claim 1, wherein building the routing matrix comprises using parallel processing to build the routing matrix.

8. The method of claim 7, further comprising determining a set of route identification operations to perform based on the routing matrix.

9. The method of claim 8, wherein the routing matrix consists of a binary number.

10. The method of claim 8, wherein route identification operations include a direct lookup operation, a longest-prefix-match lookup operation, and a hash table lookup operation.

11. The method of claim 10, wherein the at least two

routing identifiers conform to an addressing architecture defined by an Internet Engineering Task Force.

12. A machine-readable medium embodying information indicative of instructions for causing a machine to perform operations comprising:

receiving a source address and a destination address, each comprising at least two routing identifiers;

performing an EXCLUSIVE OR operation of the source address routing identifiers with the destination address routing identifiers to produce an address comparison result;

determining a set of route identification operations to perform based upon one or more non-zero values in the address comparison result, wherein a different route identification operation is to be used for each of the one or more non-zero values.

13. The machine-readable medium of claim 12, wherein the set of route identification operations comprise one or more of a direct lookup operation and a longest-prefix-match lookup operation.

14. The machine-readable medium of claim 13, wherein performing the EXCLUSIVE OR operation comprises performing an EXCLUSIVE OR operation using blocks smaller than a length

of a shortest of the destination address routing identifiers and the source address routing identifiers.

15. The machine-readable medium of claim 14, wherein the blocks comprise four-bit blocks.

16. The machine-readable medium of claim 15, wherein the destination address routing identifiers and the source address routing identifiers conform to an addressing architecture defined by an Internet Engineering Task Force.

17. A system comprising:

a processor;

a network device;

a first bus coupled with the network device and with the processor;

a memory system embodying information indicative of instructions to cause the processor to perform operations comprising receiving a source address and a destination address, each comprising at least two routing identifiers, and determining a set of route identification operations to perform based upon one or more differences between the source address routing identifiers and the destination address routing identifiers; and

a second bus coupled with the memory system and with

the processor.

18. The system of claim 17, wherein the processor comprises a parallel, hardware-based multithreaded processor.

19. The system of claim 18, wherein the network device comprises a media access controller device.

20. The system of claim 19, wherein the first bus comprises a 128-bit wide first-in-first-out bus.

21. The system of claim 18, wherein the set of route identification operations comprise one or more of a longest-prefix-match lookup operation and one or more direct lookup operations.

22. The system of claim 21, wherein the memory system comprises a dynamic random access memory and a static random access memory.

23. The system of claim 22, wherein the second bus comprises a peripheral component interconnect bus.

24. A communication system comprising:

a processor;

means for receiving a source address and a destination address, each comprising at least two routing identifiers;

means for using the processor to identify one or more differences between the source address routing identifiers and the destination address routing identifiers;

means for determining a set of route identification operations based upon the one or more differences, wherein a different route identification operation is determined for each of the one or more differences; and

means for routing data based upon the set of route identification operations.

25. The system of claim 24, wherein the processor comprises a parallel, hardware-based multithreaded processor.